دانشگاه صنعتی امیرکبیر

دانشکده مهندسی برق

طراحی مدارهای VLSI

فصل هفتم: مدار های ترتیبی

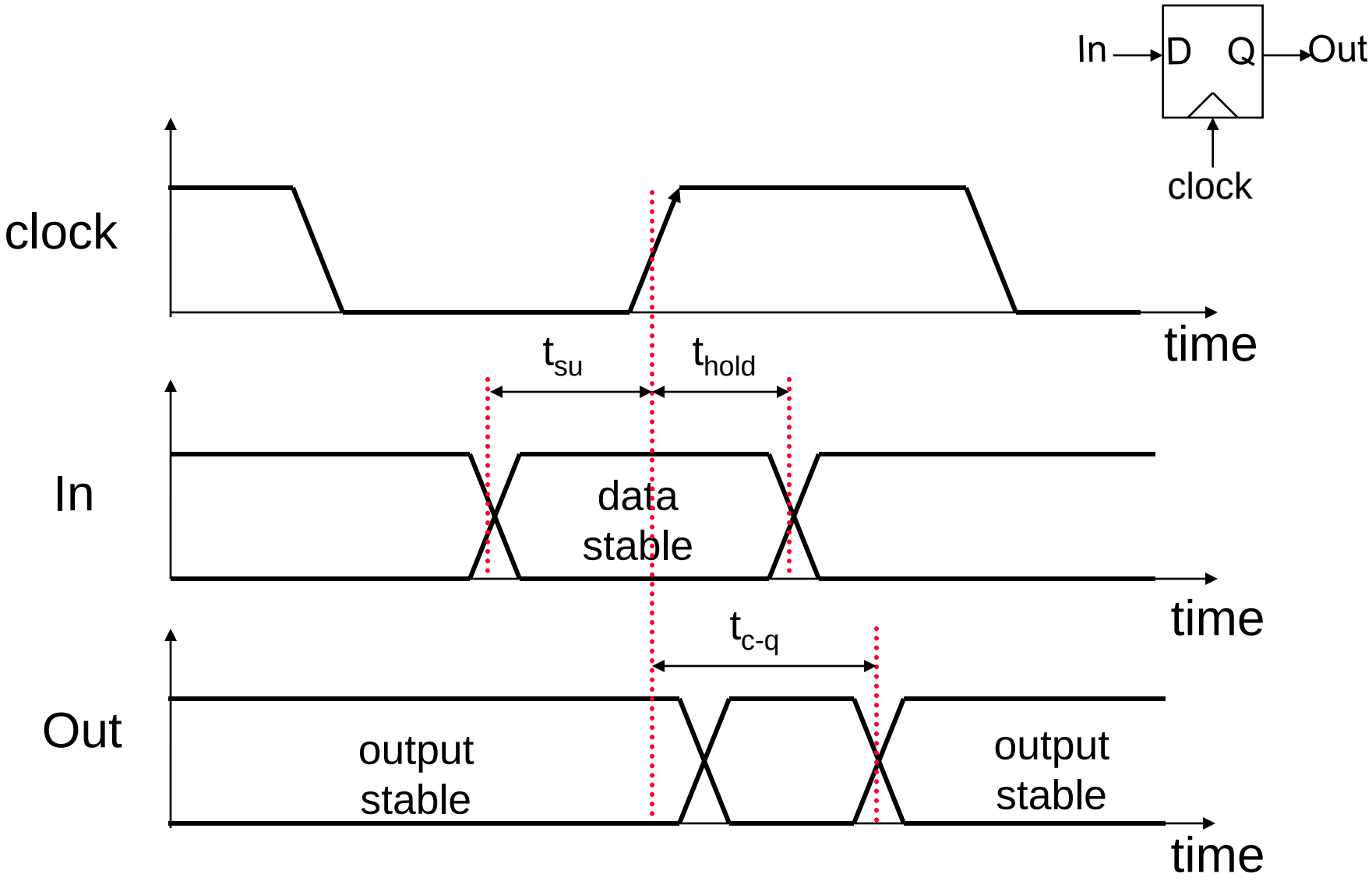
بخش دوم : مدار های ترتیبی پویا

مجید شالچیان

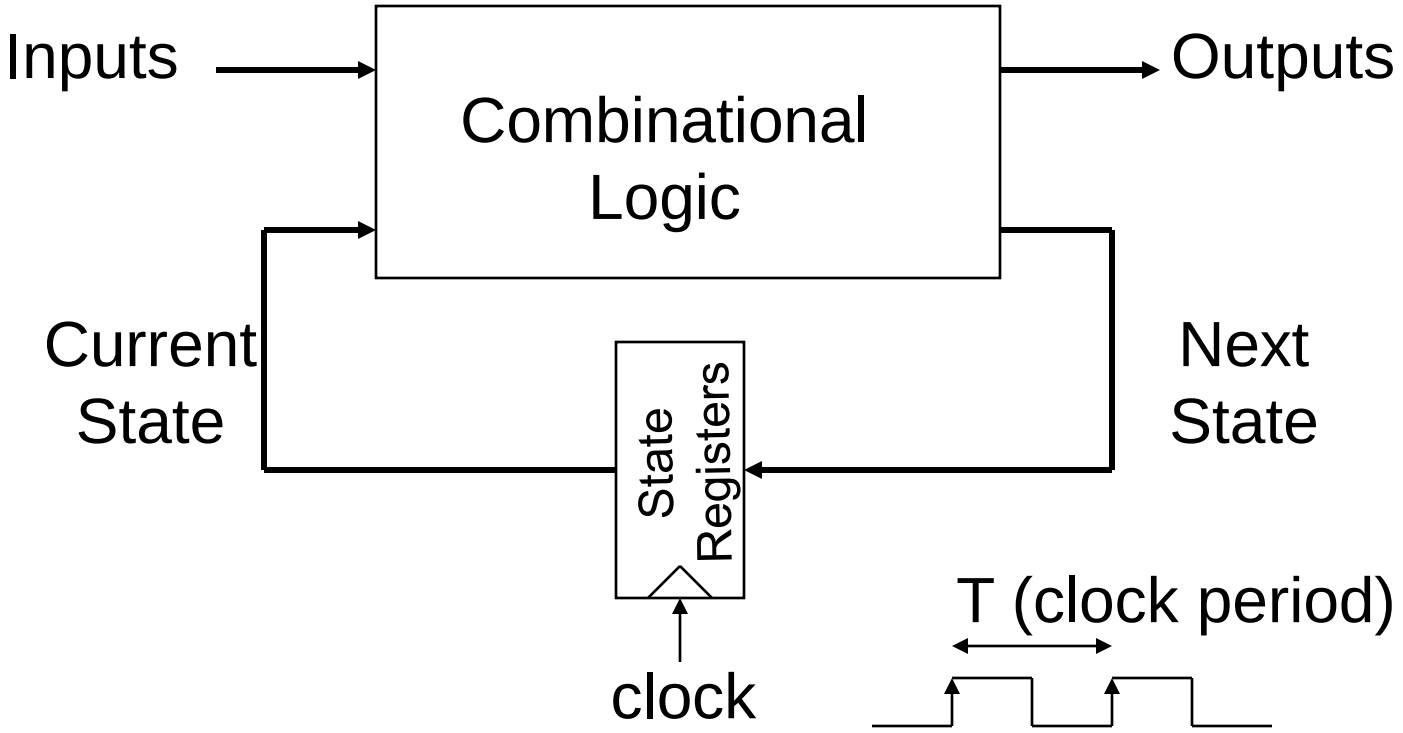
رجیستر های ایستا و پویا

- رجیستر های ایستا
  - حالت را تا زمانیکه منبع تغذیه روشن است نگهداری می کنند.
  - مبتنی بر وجود حلقه فیدبک مثبت بین خروجی و ورودی عمل می کنند.
  - وقتی تغییرات سیگنال چندان سریع نیست می توان با clock gating توان را کم کرد.
- رجیستر های پویا
  - حالت در خازنهای پارازیتی ذخیره می شود.
  - برای زمان های بسیار کوتاه (میلی ثانیه) حالت را ذخیره می کنند.
  - نیاز به بازسازی متناوب سیگنال دارند (Refresh)
  - معمولا ساده تر دارای سرعتبالاتر و مصرف توان کمتر هستند.

یادآوری Timing Metrics



Review: System Timing Constraints

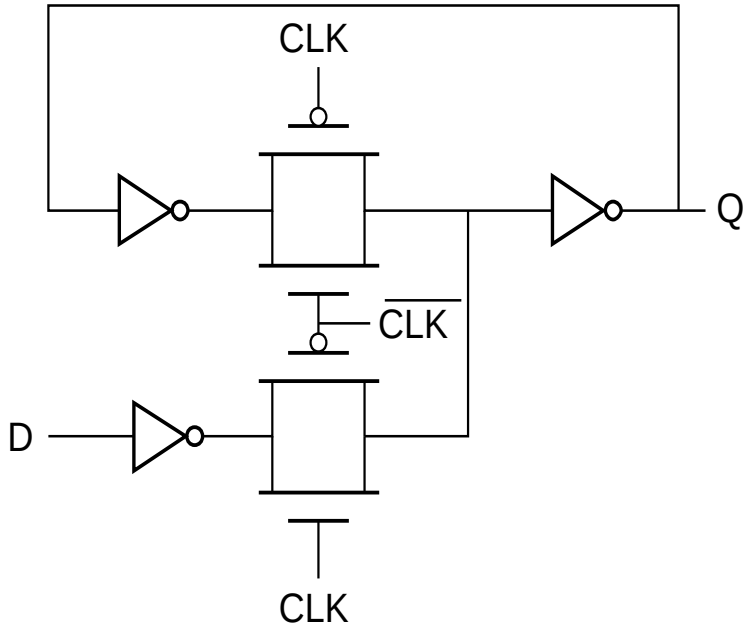


$$t_{cdreg} + t_{cdlogic} \geq t_{hold}$$

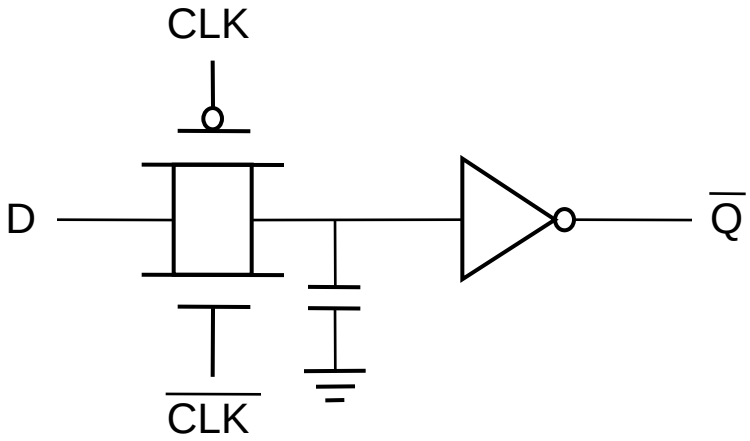
$$T \geq t_{c\text{-}q} + t_{plogic} + t_{su}$$

مقایسه لچ ایستا و پویا

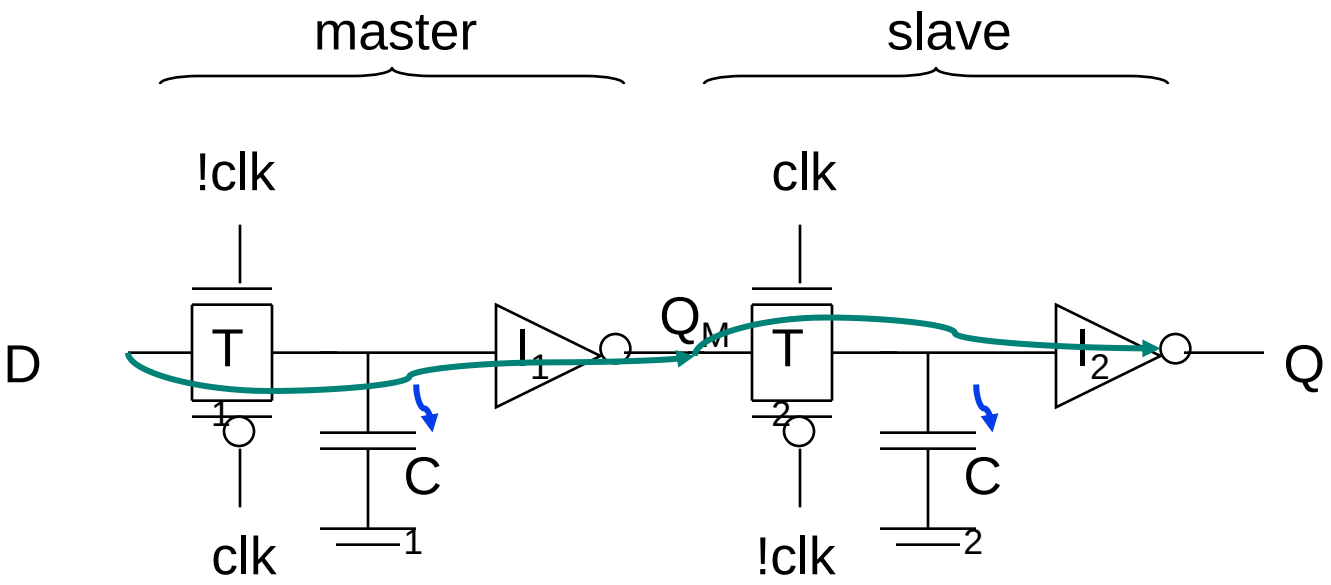
Static



Dynamic (charge-based)



فلیپ فلاپ حساس به لبه دینامیکی

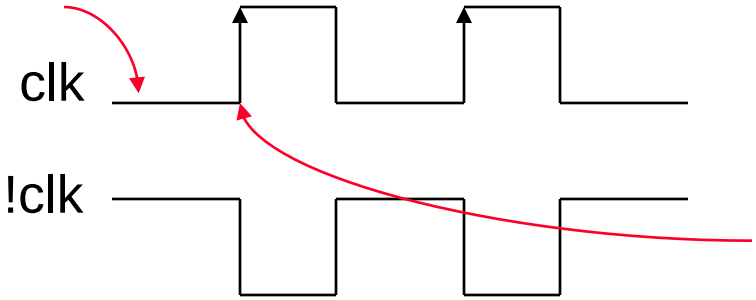


$t_{su} = t_{pd\_tx}$

$t_{hold} = zero$

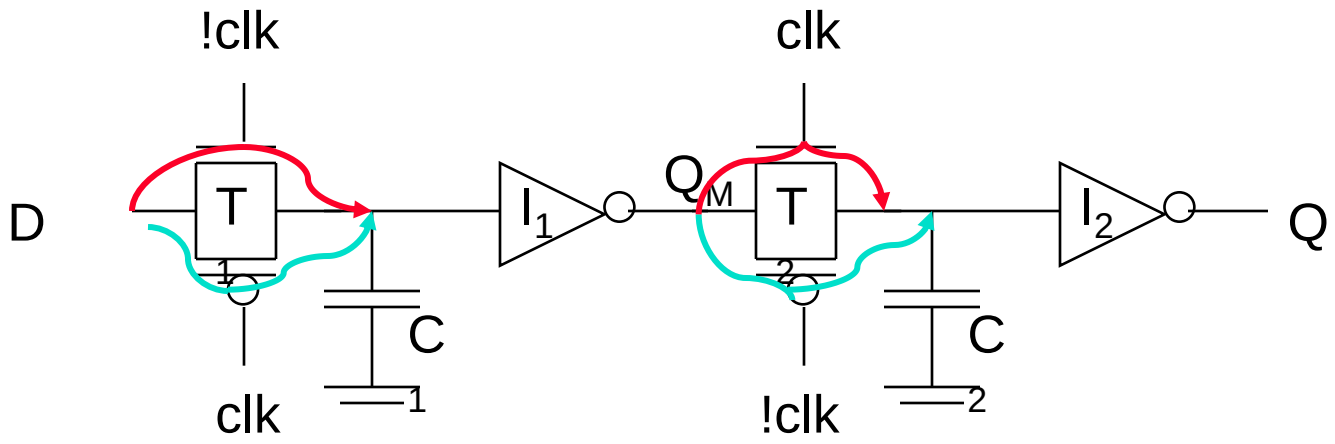
$t_{c\text{-}q} = 2\,t_{pd\_inv} + t_{pd\_tx}$

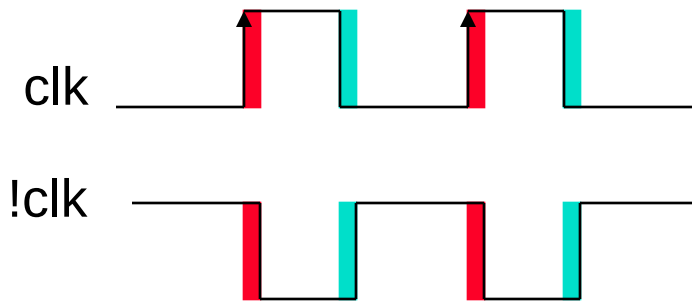
master transparent
slave hold



master hold
slave transparent

همپوشانی کلاک و race condition





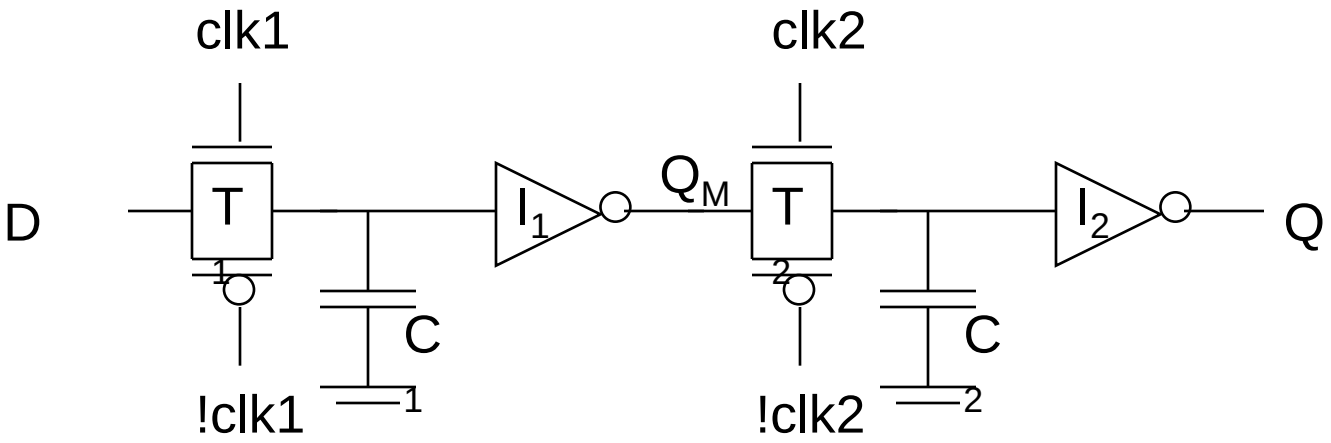
0-0 overlap race condition

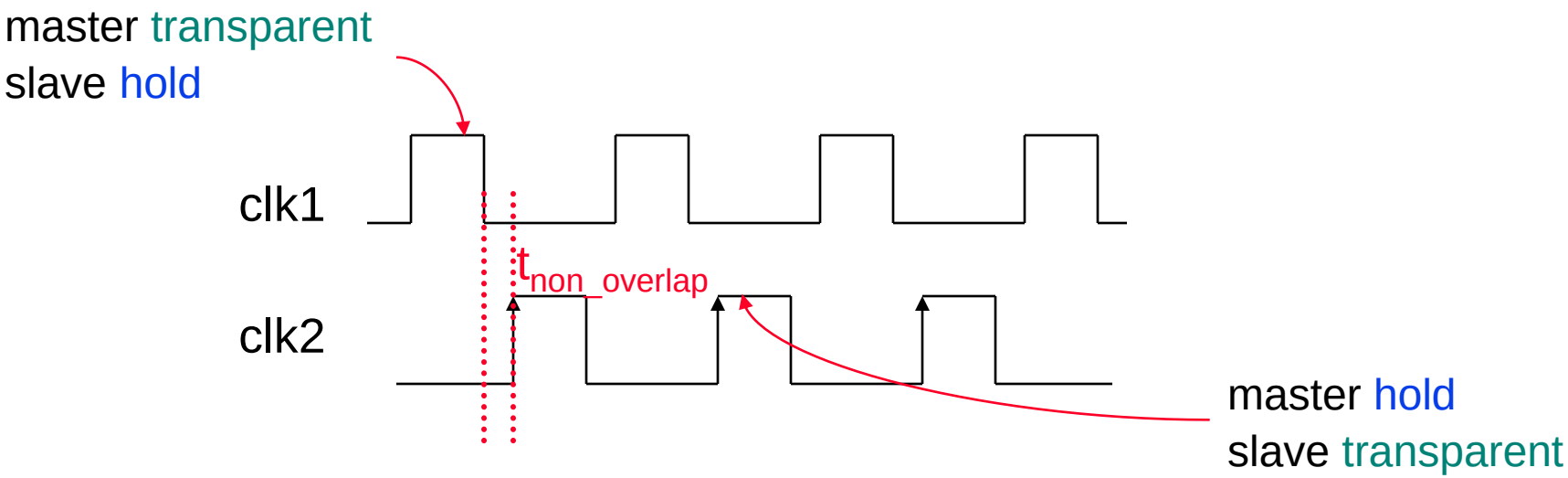
$t_{overlap0\text{-}0} < t_{T1} + t_{I1} + t_{T2}$

1-1 overlap race condition

$t_{overlap1\text{-}1} < t_{hold}$

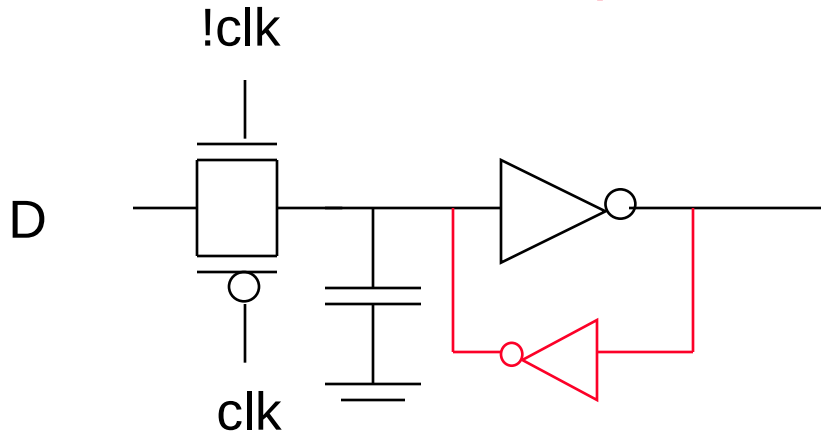
استفاده از کلاک های نا همپوشان





Pseudostatic Dynamic Latch

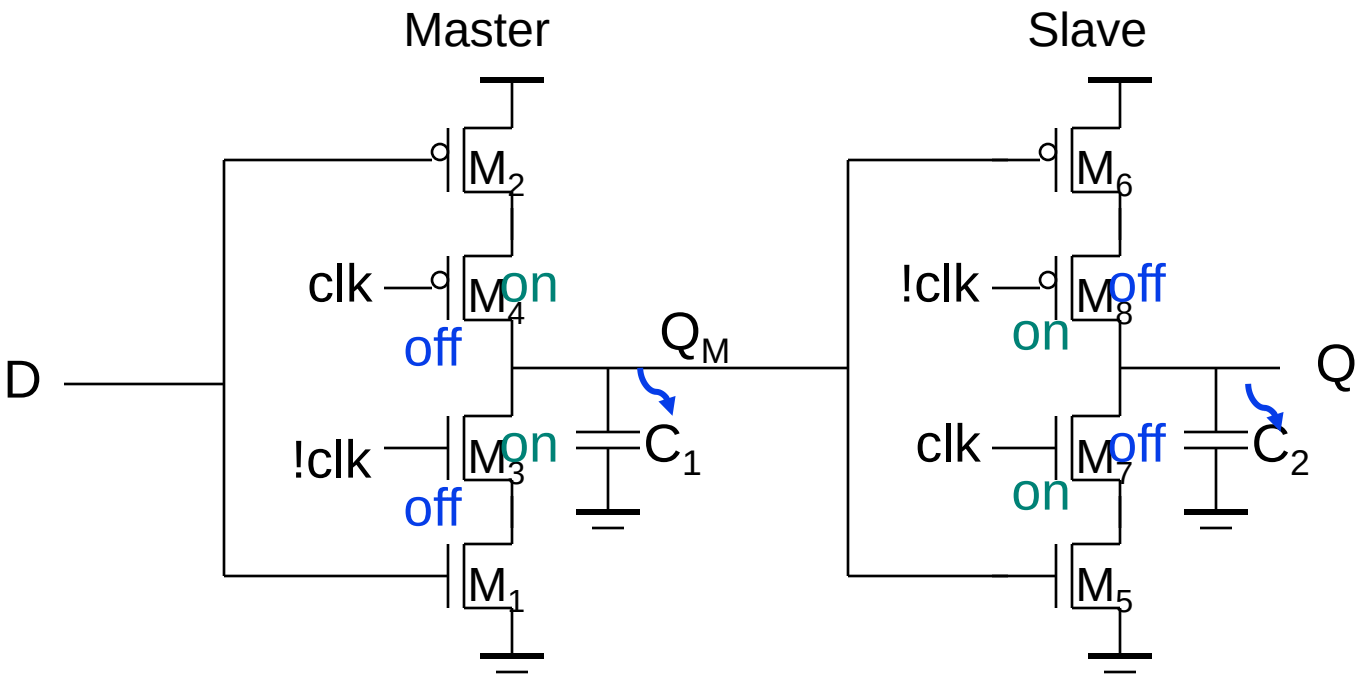
- Robustness considerations limit the use of dynamic FF's
  - coupling between signal nets and internal storage nodes can inject significant noise and destroy the FF state
  - leakage currents cause state to leak away with time
  - internal dynamic nodes don't track fluctuations in V_{DD} that reduces noise margins
- A simple fix is to make the circuit pseudostatic



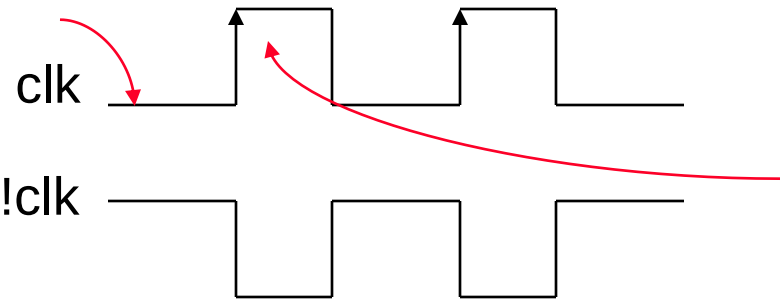
- Add above logic added to all dynamic latches

C²MOS (Clocked CMOS) ET Flipflop

- A clock-skew insensitive FF



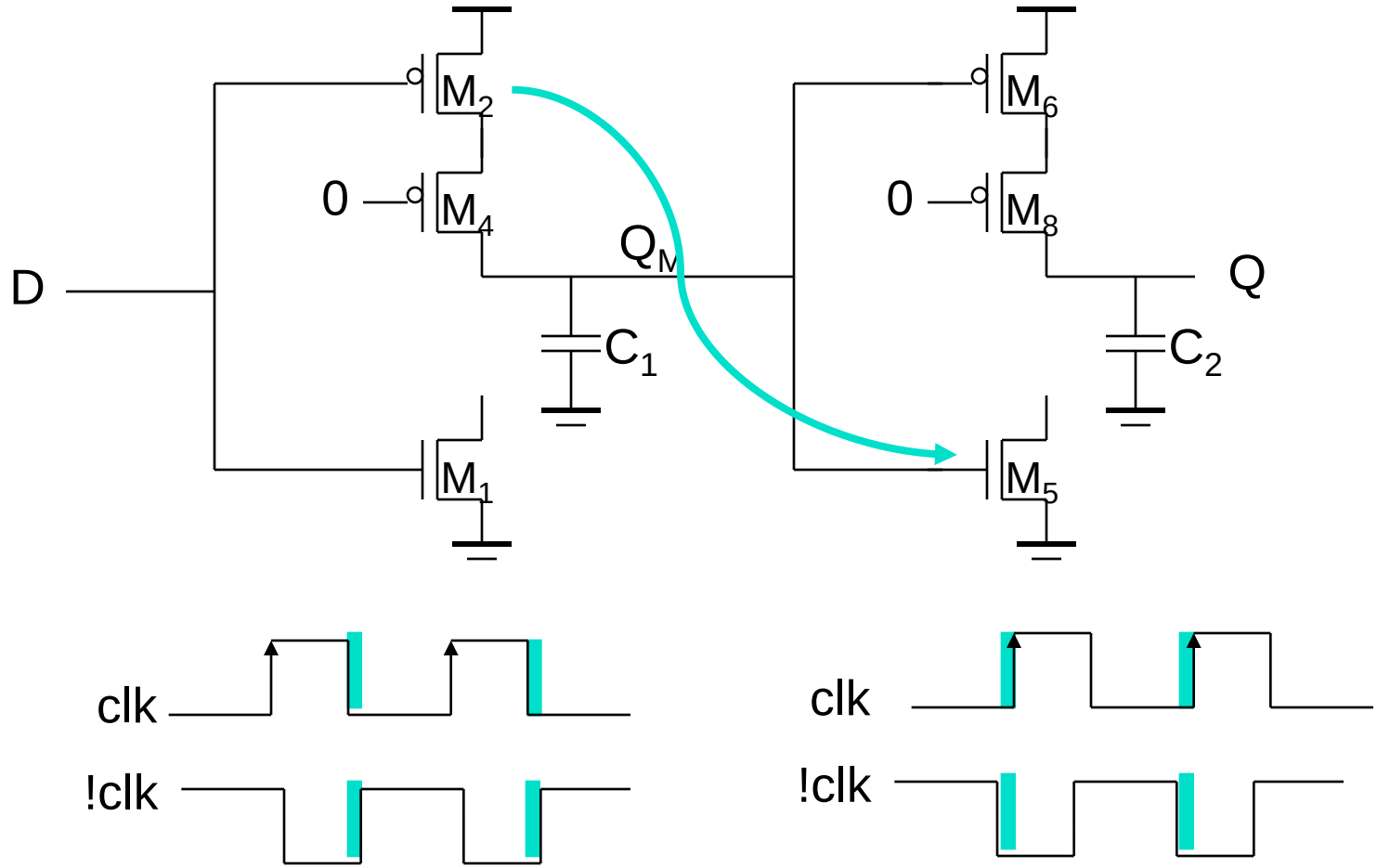
master transparent
slave hold



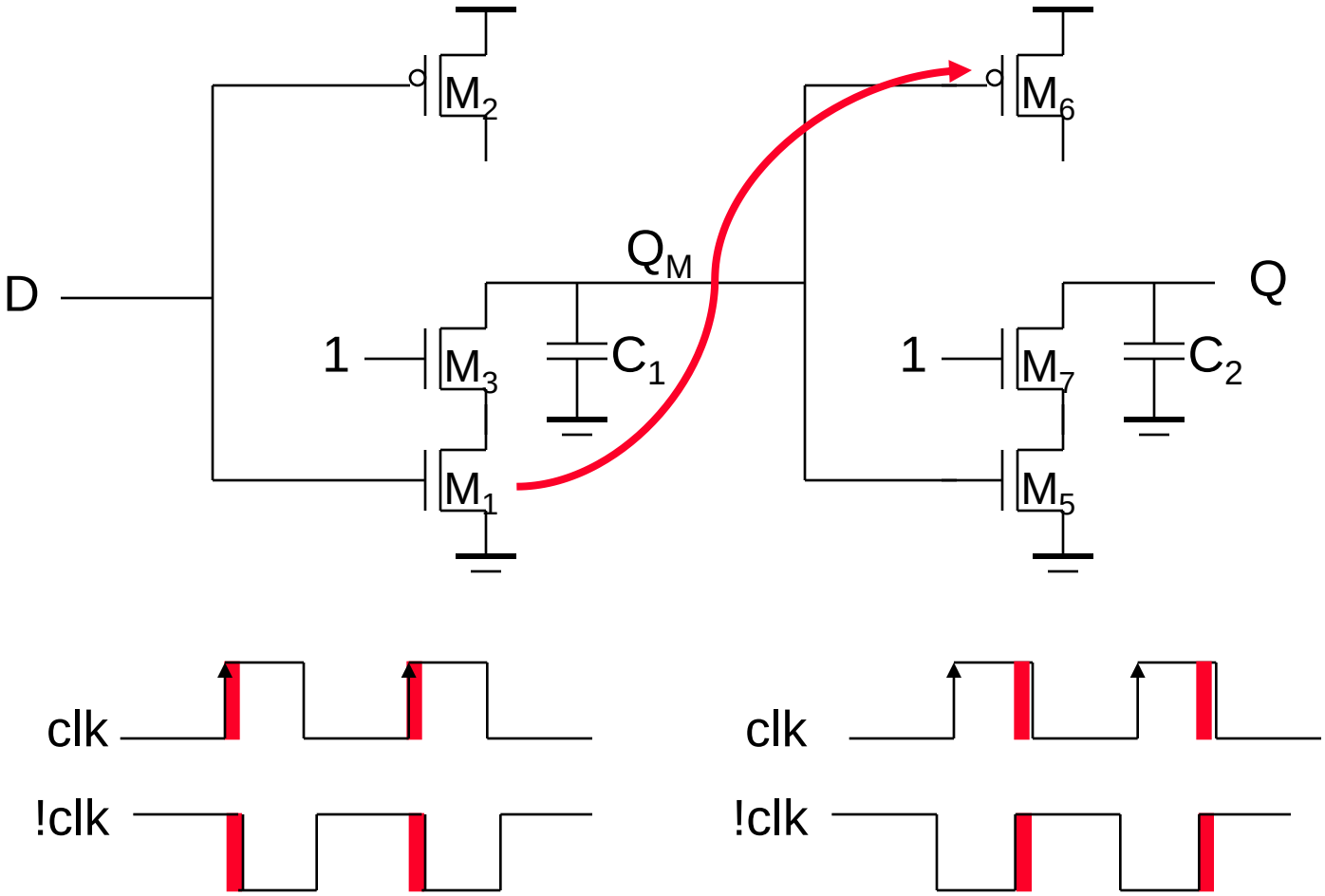
master hold
slave transparent

C²MOS FF 0-0 Overlap Case

- Clock-skew insensitive as long as the rise and fall times of the clock edges are sufficiently small



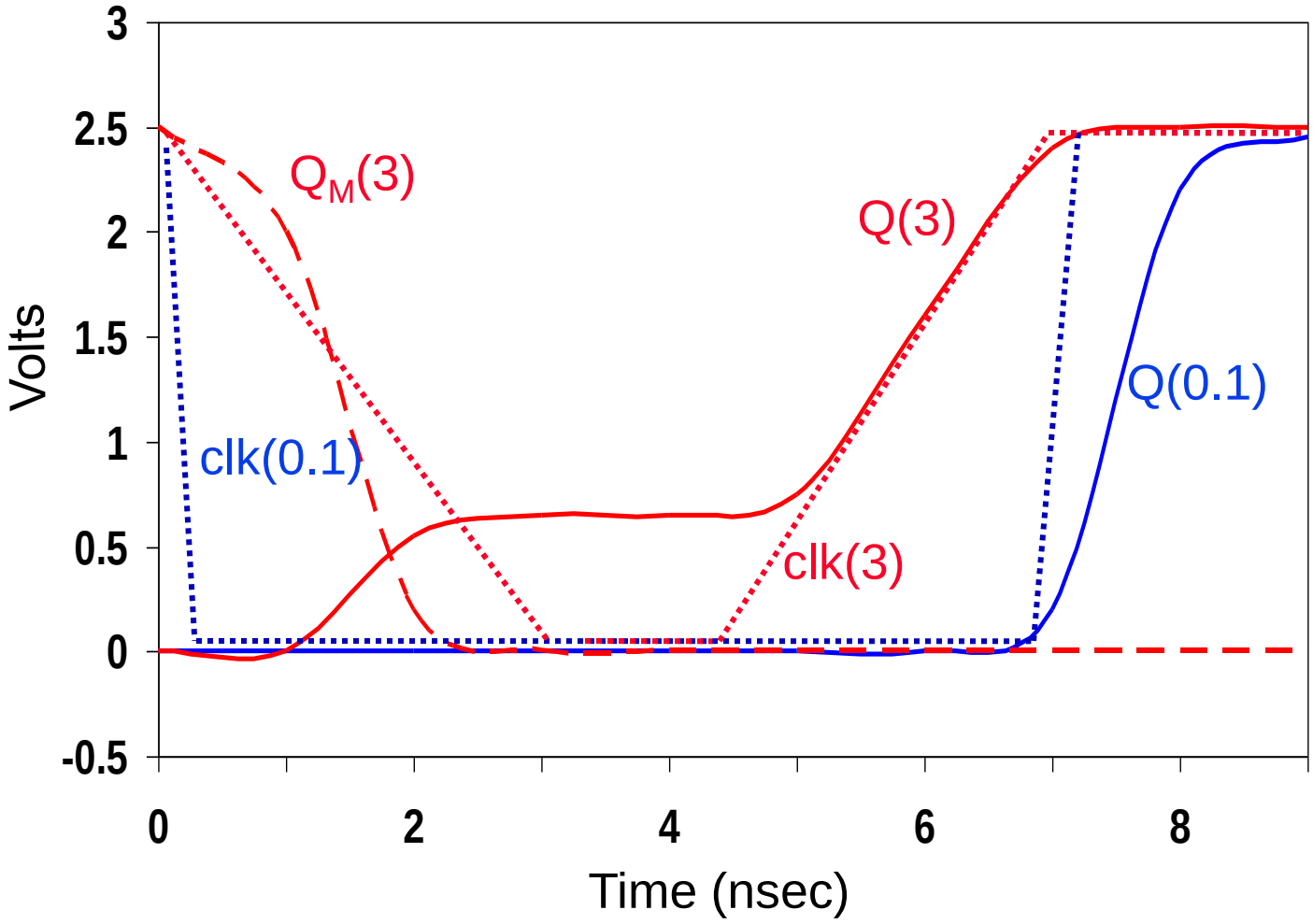
C²MOS FF 1-1 Overlap Case



1-1 overlap constraint

$t_{overlap1\text{-}1} < t_{hold}$

C²MOS Transient Response

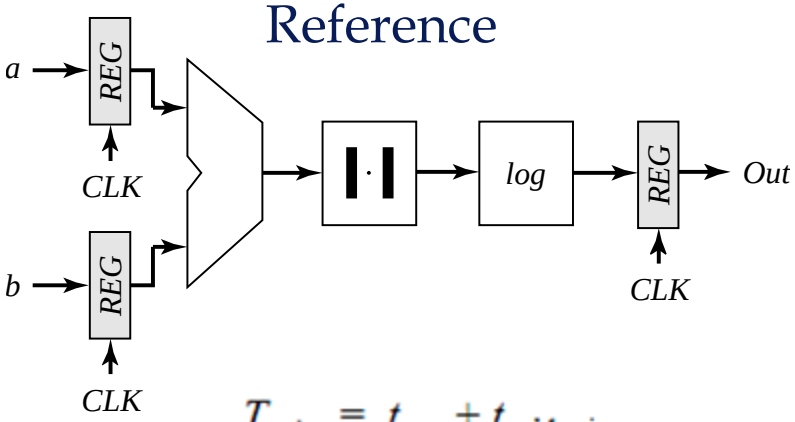


For a
0.1 ns clock

For a
3 ns clock
(race condition
exists)

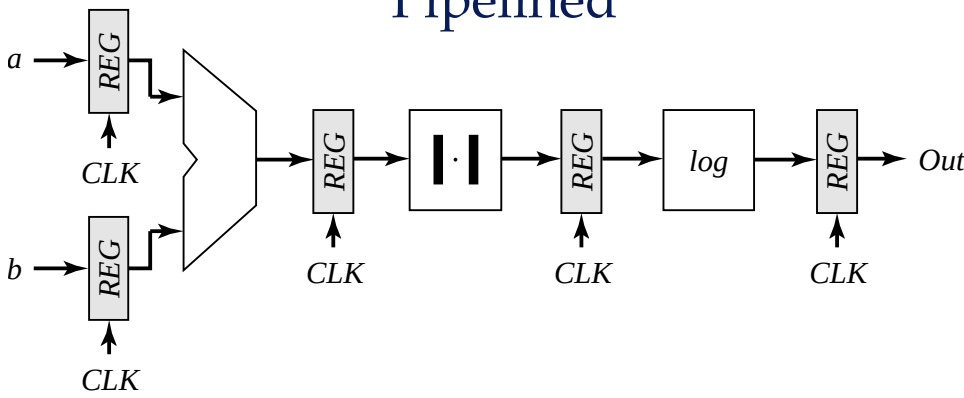
Pipelining

Reference



$$T_{min} = t_{c\text{-}q} + t_{pd,\text{logic}}$$

Pipelined



$$T_{min,\text{pipe}} = t_{c\text{-}q} + \max(t_{pd,\text{add}}, t_{pd,\text{abs}}, t_{pd,\text{log}})$$

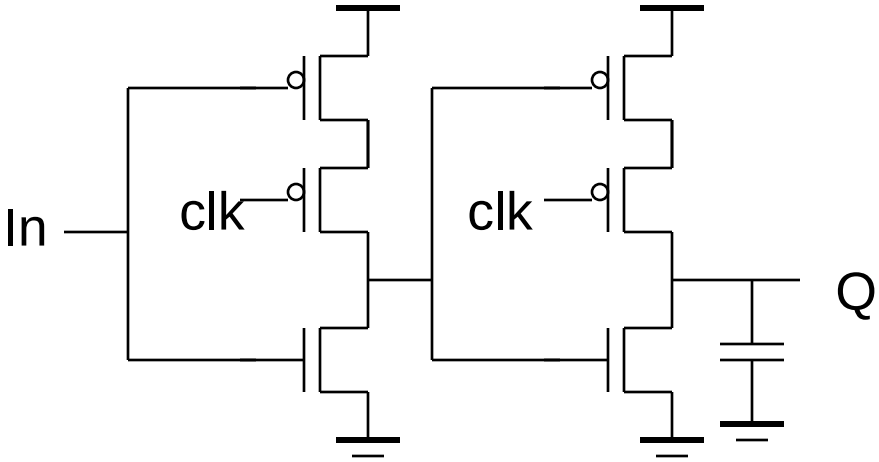
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\lvert a_1 + b_1 \rvert$	
3	$a_3 + b_3$	$\lvert a_2 + b_2 \rvert$	$\log(\lvert a_1 + b_1 \rvert)$
4	$a_4 + b_4$	$\lvert a_3 + b_3 \rvert$	$\log(\lvert a_2 + b_2 \rvert)$
5	$a_5 + b_5$	$\lvert a_4 + b_4 \rvert$	$\log(\lvert a_3 + b_3 \rvert)$

Operation modes for NORA logic modules.

	CLK block		*CLK* block	
	Logic	**Latch**	**Logic**	**Latch**
$CLK = 0$	Precharge	Hold	Evaluate	Evaluate
$CLK = 1$	Evaluate	Evaluate	Precharge	Hold

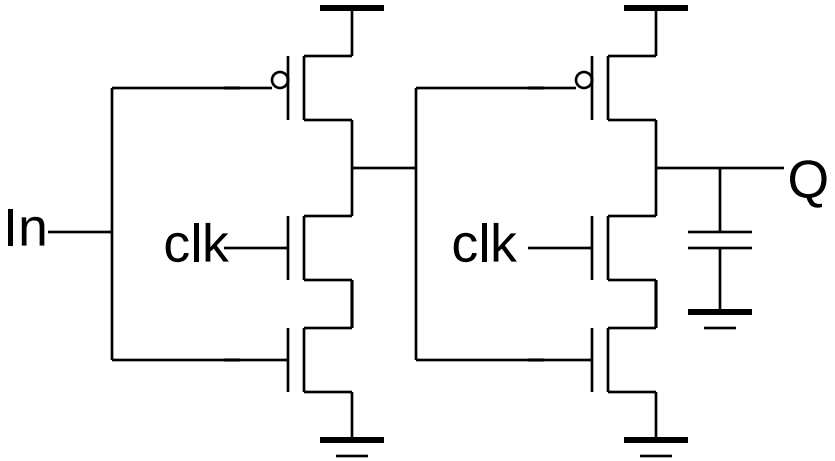
True Single Phase Clocked (TSPC) Latches

Negative Latch



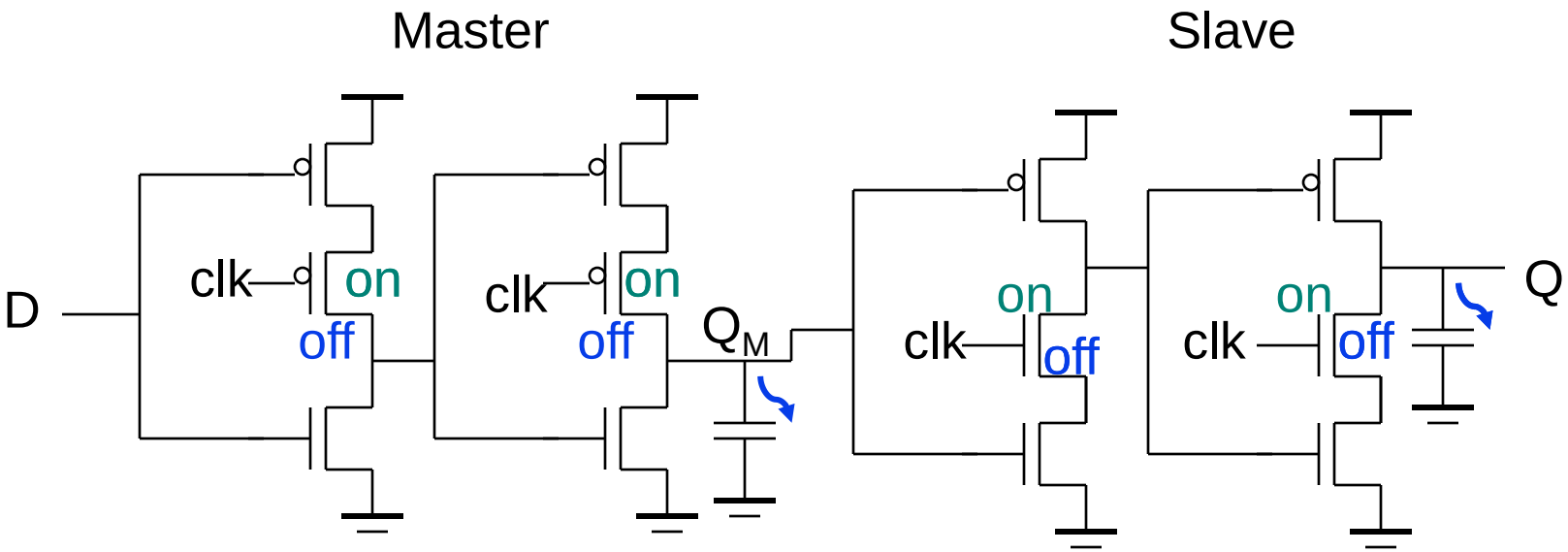
hold when clk = 1
transparent when clk = 0

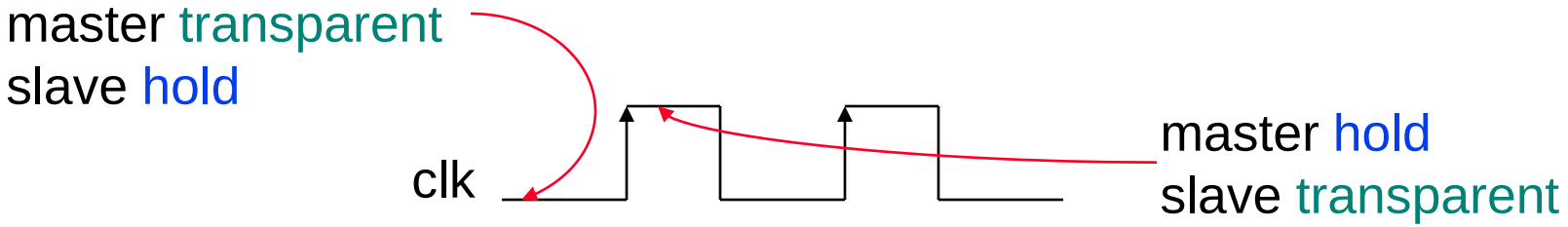
Positive Latch



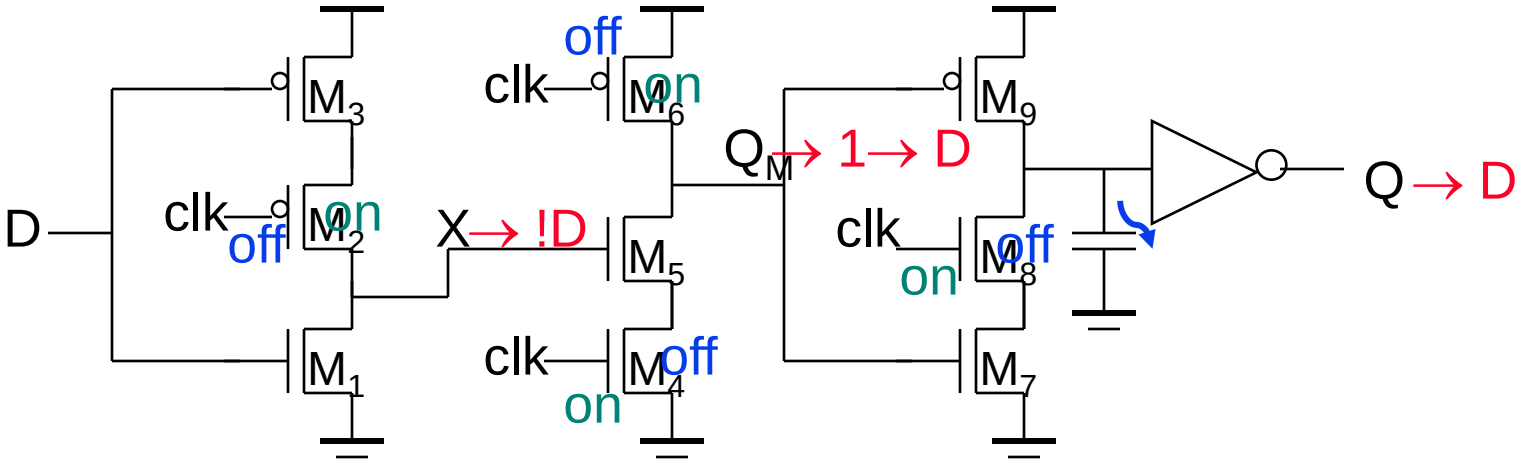
transparent when clk = 1
hold when clk = 0

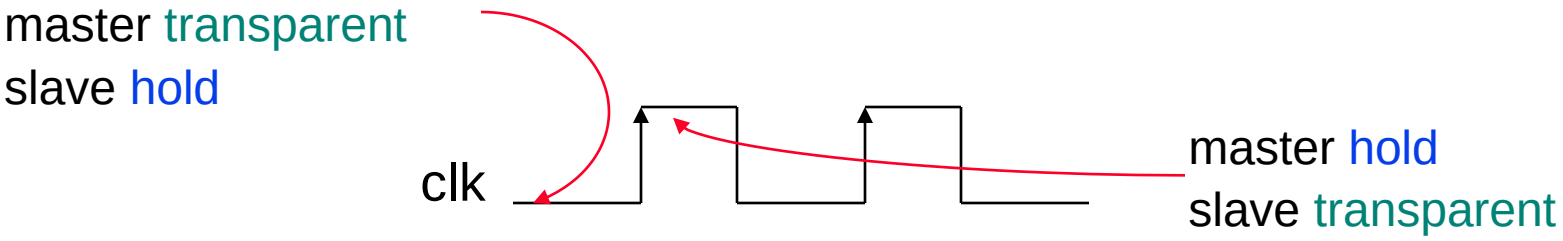
TSPC ET FF


Master
Slave
D
clk
on
off
clk
on
off
Q_M
on
clk
off
on
clk
off
Q

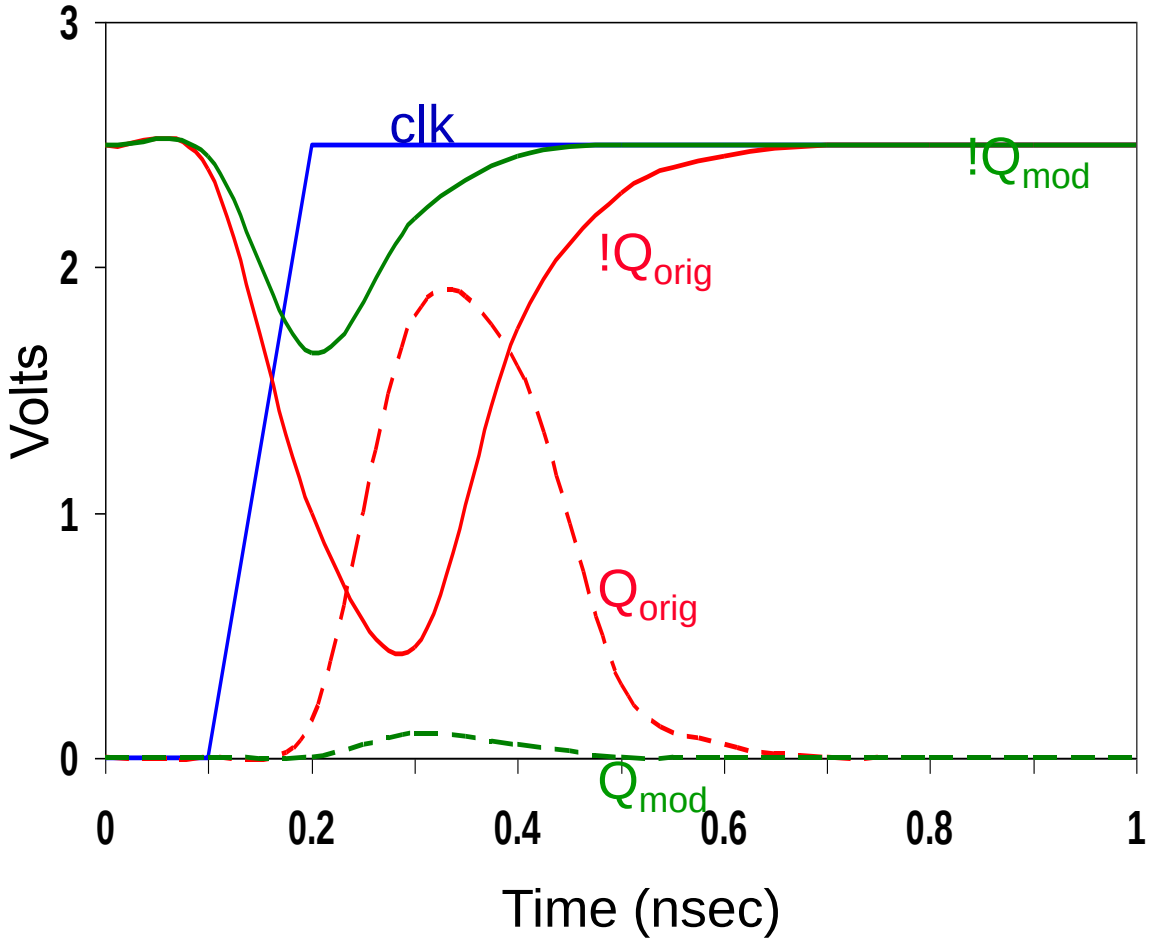

master transparent
slave hold
clk
master hold
slave transparent

Simplified TSPC ET FF





Sizing Issues in Simplified TSPC ET FF



Transistor sizing

Original width

M_4, M_5 = 0.5μm

M_7, M_8 = 2μm

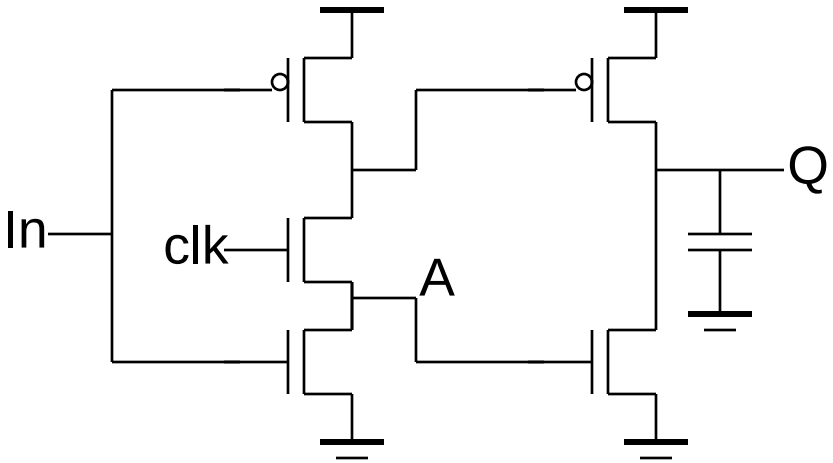
Modified width

M_4, M_5 = 1μm

M_7, M_8 = 1μm

Split-Output TSPC Latches

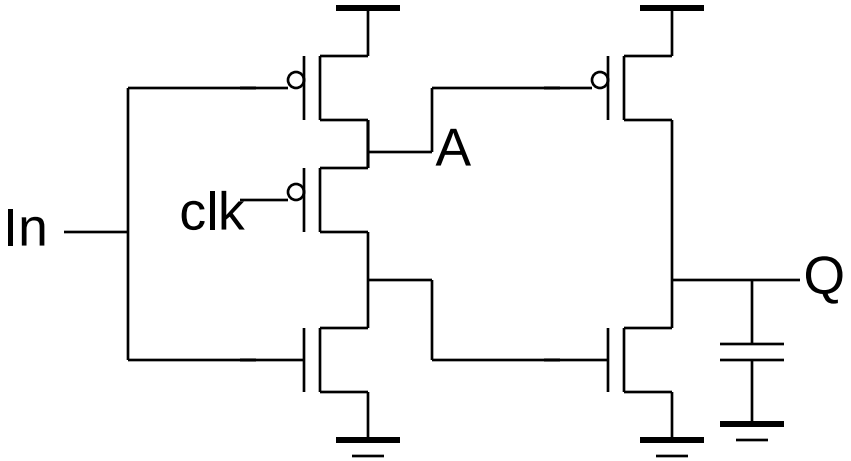
Positive Latch



transparent when clk = 1
hold when clk = 0

When In = 0, A = $V_{DD} - V_{Tn}$

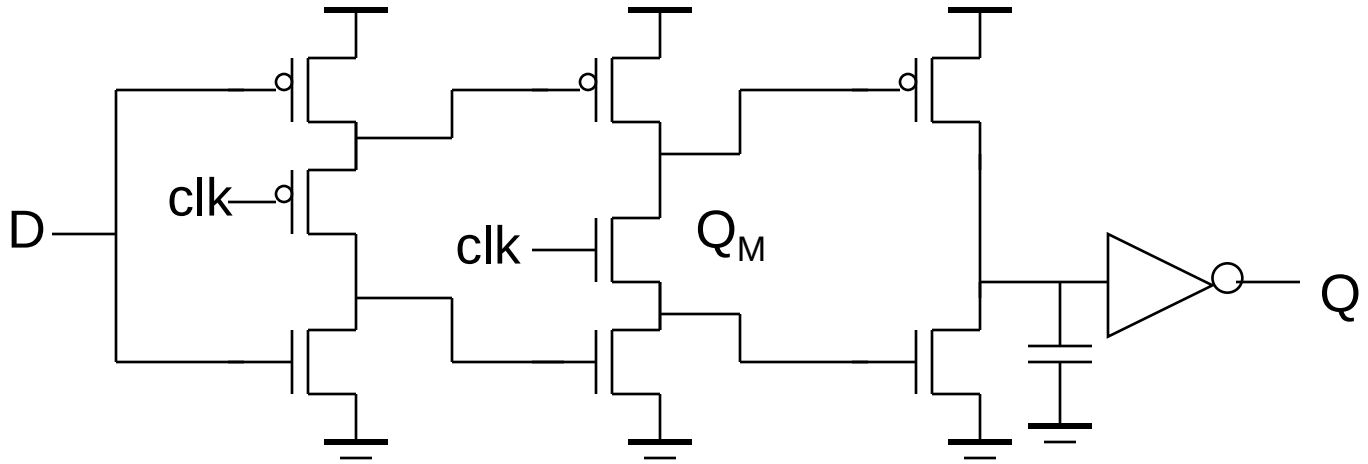
Negative Latch

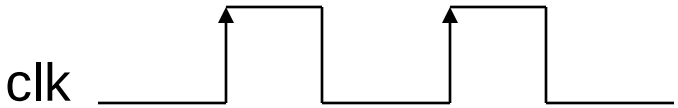


hold when clk = 1
transparent when clk = 0

When In = 1, A = $|V_{Tp}|$

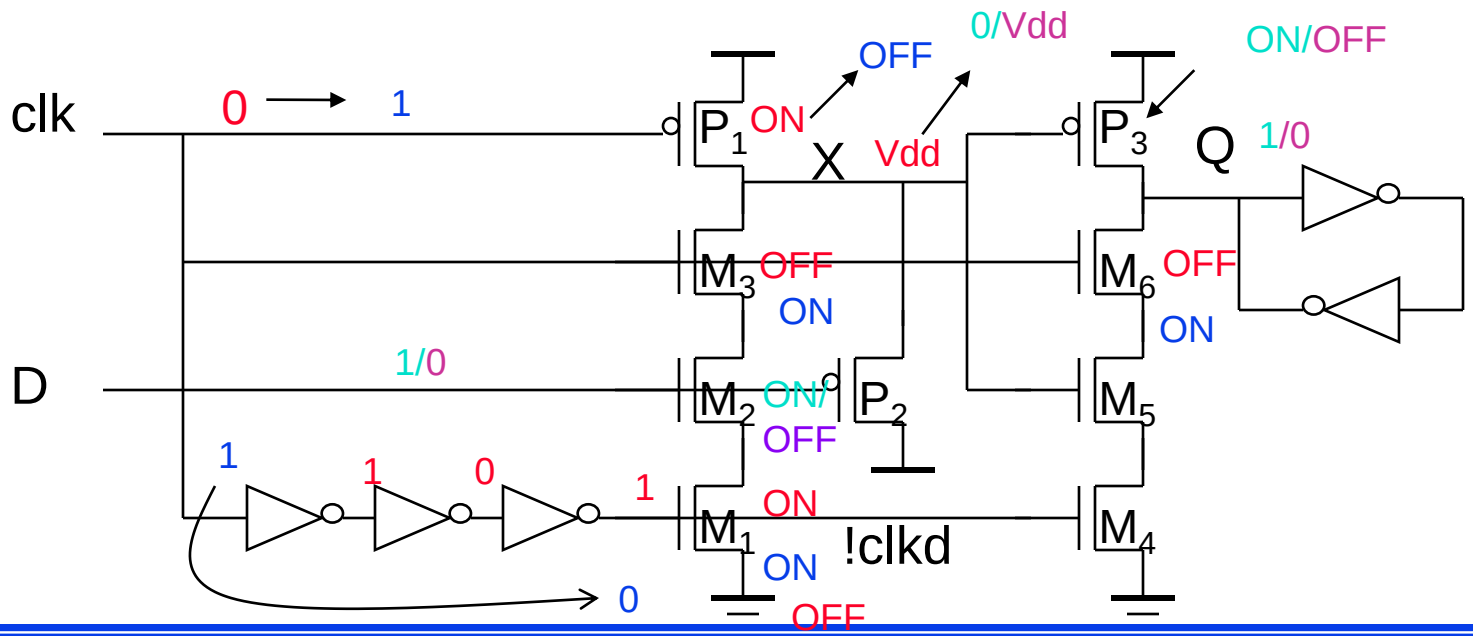
Split-Output TSPC ET FF





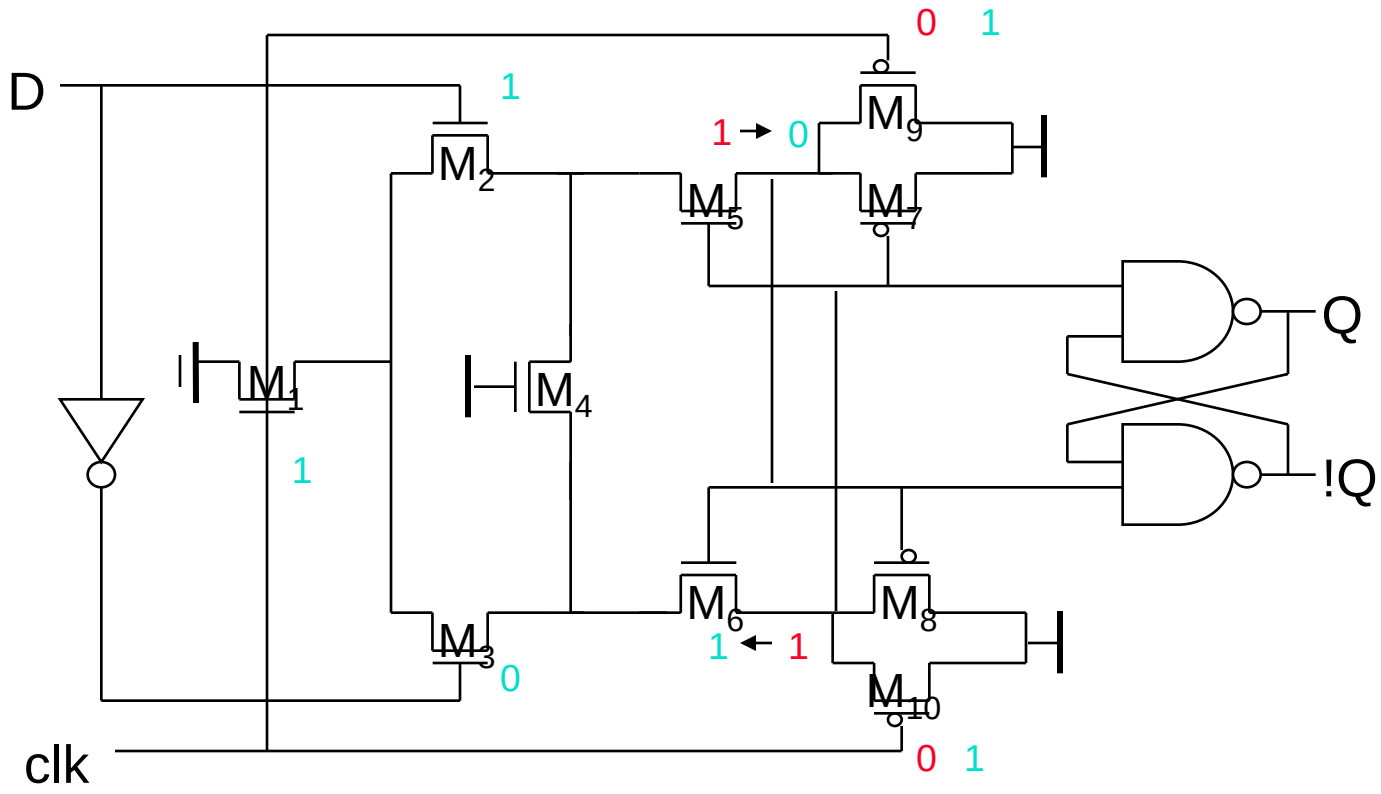
Pulsed FF (AMD-K6)

- Pulse registers - a short pulse (glitch clock) is generated locally from the rising (or falling) edge of the system clock and is used as the clock input to the flipflop
  - race conditions are avoided by keeping the transparent mode time very short (during the pulse only)
  - advantage is reduced clock load; disadvantage is substantial increase in verification complexity



Sense Amp FF (StrongArm SA100)

- Sense amplifier (circuits that accept small swing input signals and amplify them to full rail-to-rail signals) flipflops
  - advantages are reduced clock load and that it can be used as a receiver for reduced swing differential buses



Flipflop Comparison Chart

Name	Type	#clk ld	#tr	t_{set-up}	t_{hold}	t_{pFF}
Mux	Static	8 (clk-!clk)	20	$3t_{pinv}+t_{ptx}$	0	$t_{pinv}+t_{ptx}$
PowerPC	Static	8 (clk-!clk)	16			
2-phase	Ps-Static	8 (clk1-clk2)	16			
T-gate	Dynamic	4 (clk-!clk)	8	t_{ptx}	t_{o1-1}	$2t_{pinv}+t_{ptx}$
C^2MOS	Dynamic	4 (clk-!clk)	8			
TSPC	Dynamic	4 (clk)	11	t_{pinv}	t_{pinv}	$3t_{pinv}$
S-O TSPC	Dynamic	2 (clk)	10			
AMD K6	Dynamic	5 (clk)	19			
SA 100	SenseAmp	3 (clk)	20			

Choosing a Clocking Strategy

- Choosing the right clocking scheme affects the functionality, speed, and power of a circuit
- Two-phase designs
  - + robust and conceptually simple
  - - need to generate and route two clock signals
  - - have to design to accommodate possible skew between the two clock signals
- Single phase designs
  - + only need to generate and route one clock signal
  - + supported by most automated design methodologies
  - + don't have to worry about skew between the two clocks
  - - have to have guaranteed slopes on the clock edges